

Comprehensive DRAM (DDR5/LPDDR6) Architecture Course Info

Let MindShare Bring “DRAM (DDR_x/LPDDR_x) Architecture” to Life for You

Whether you are new to DRAM or an industry veteran seeking the latest and greatest standards, you will learn more than you expect from MindShare's DRAM courses. You may be well-versed on modern serial protocols but learning parallel-bus protocols of DDR DRAM will be valuable. You might have worked extensively with mainstream PC DRAMs and now you need to learn low-power LP DRAM designs. This DRAM course will help you design, develop, validate, verify, test, debug or support DRAM interfaces.

You Will Learn:

- Where JEDEC expects DRAM to appear in a system
- How a DRAM cell is addressed by the controller
- Difference between Banks, Bank Groups and Ranks
- Why the DRAM controller is so complicated
- Activation, Precharge and Refresh including newer forms
- DDR4 as fundamental technology
- Types of DIMMs
- Fly-By Routing
- DDR5, LPDDR5 and LPDDR6 pin definitions, bank state diagrams and timing waveforms
- DDR5 DIMM PMIC
- Dynamic Voltage and Frequency Scaling (DVFS), Frequency Set Points (FSP) and clock throttling
- On-Die Termination (ODT)
- JEDEC Initialization and Mode Registers
- Calibration and training
- Sources of errors and JEDEC features for handling errors
- Test philosophy and JEDEC features to assist with testing

Course Length: 4 Days

Who Should Attend?

This course is hardware-centric and describes initialization and training of DRAM devices and controllers. It is suitable for hardware engineers though software/firmware engineers will benefit. The course is ideal for DRAM controller designers, chipset designers, system board-level design and validation engineers. The course introduces current DRAM technologies with DDR4 as a baseline to teach concepts that are common to all DRAMs. The course covers in detail all new features of DDR5, LPDDR5, and LPDDR6.

Course Contents:

- System Architecture
 - PC Platform Architecture
 - NUMA Architecture
 - SoC Architecture
- Back to the Future DRAM Intro
 - It's more similar than it is different
- DRAM Cell Architecture
 - Problems of Activation, Precharge and Refresh
- DRAM Device Architecture
 - SDRAM through DDR5 and LPDDR6
 - Bank Groups
 - LPDDR5 Bank Group options

- Packaging
 - Monolithic
 - Stacked Die
 - 3DS, Hybrid Memory Cube, High Bandwidth Memory (HBM)
 - Package-on-Package
 - Dual LPDDR4 Channels
- DRAM Controller Basics
 - Functional Blocks
 - Address Translation/Address Mapping Examples
- Device and Dual In-line Memory Module (DIMM) Pin Descriptions
 - DDR4
 - DIMM
- Introduction to DIMM Architecture
 - UDIMM
 - RDIMM
 - LRDIMM
 - Fly-by Routing
- Bank State Machines, Commands, Waveforms
 - DDR4
- Refresh
 - Auto Refresh
 - Self Refresh
 - Auto Self Refresh
- Rowhammer Mitigations
 - Target Row Refresh
 - Refresh Management
 - Per-Row Activation Count
- Device and DIMM Pin Descriptions
 - DDR5
 - DIMM
 - LPDDR5
 - LPDDR6
- DDR4 and DDR5 DIMM Architecture
 - UDIMM
 - RDIMM
 - LRDIMM
 - PMIC
 - DDR4 On-DIMM Address Mirroring
 - DDR5 Mirroring
- Bank State Machines, Commands, Waveforms
 - DDR5
 - LPDDR5 and LPDDR6
- Newer Forms of Refresh
 - Per-Bank and Fine Granularity Refresh
 - Temperature Compensated Refresh
 - Self-Refresh Abort, Fast Exit
- Electrical Specifications
 - DDR4/DDR5 POD
 - LPDDR5/LPDDR6 LVSTL
 - IDD Specifications, Example

- Power Management
 - Power Down and Self Refresh
 - DDR4/DDR5 Max Power Saving Mode
 - LPDDR5/LPDDR6 Frequency Setpoints (FSP)
 - LPDDR5/LPDDR6 Dynamic Voltage and Frequency Scaling
 - DVFSC, DVFSH, DVFSL, DVFSB, DVFSQ
- Introduction to Signal Integrity Issues
 - Sources and Solutions
- On-Die Termination
 - Sync/Async ODT
 - DDR4/DDR5/LPDDR6 Dynamic ODT
 - Data Group ODT and Command Bus ODT
 - DDR4/DDR5/LP DRAM Park Mode
 - Command Bus ODT
- Initialization, Calibration and Training
 - JEDEC Initialization
 - DDR4 Mode Registers
 - DDR4 Initialization
 - DDR5, LPDDR5, LPDDR6 Initialization
 - Calibration and Training
 - ZQ Calibration
 - Vref Training
 - CS Training Mode
 - CA Command Bus Training
 - Write Leveling
 - Read Calibration
 - Write Calibration
 - Duty Cycle Adjustment, Duty Cycle Monitor, DFE, FIFO, DQS Oscillator
- Errors and Error Handling
 - Sources of Errors
 - DIMM ECC
 - On-Die ECC
 - DIMM Parity
 - DDR4 CA Parity
 - DDR4 Write CRC
 - DDR5 Read/Write CRC
 - LPDDR5/LPDDR6 Link ECC/EDC
 - LPDDR6 In-line ECC with System Metadata Carve Out
 - Post Package Repair
- Testing
 - DRAM Functional Tests
 - Structural Test Example
 - Cell Test Example
 - DRAM Parametric (pin) Tests
 - DDR4 Connectivity Test Mode
 - DDR5 Loopback Mode
 - LPDDR6 Loopback Mode
- Optional Topics
 - SMBus Overview, I3C
 - NVM Transaction Overview

Recommended Prerequisites:

A basic understanding of digital design and some computer architecture background.

Course Material:

- Students will be provided a softcopy of the presentation materials used in class.
- DRAM (DDRx/LPDDRx) Architecture eLearning course

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