

Ultra Accelerator Link (UALink) Architecture Fundamentals

Let MindShare Bring “Ultra Accelerator Link (UALink) Architecture Fundamentals” to Life for You

The UALink specification outlines a set of protocols and interfaces designed to form systems using multiple System Nodes aimed at AI applications. Each System Node normally includes one or more Host CPUs and Accelerators connected by various interconnects such as CXL, PCIe, AMD Infinity Fabric, etc. These nodes typically allow coherent access across Host and Accelerator memory within the node. Each node operates under a single OS image. UALink supports low-latency communication between Accelerators across System Nodes, allowing direct read, write, and atomic transactions. This inter-node communication is restricted to Accelerator initiated traffic. UALink protocol does not permit Host CPU access to memory across different System Nodes.

The UALink specification defines the UALink interface between different physical devices connected by a Link. The specification not only includes the traditional description of a serial bus stack (Transaction, Data Link and Physical Layer), but also includes a description of a UALink Protocol Level Interface (UPLI) also referred to as the Protocol Layer. The UPLI facilitates the standardization of an interface between a component and the UALink stack whether the component be an Accelerator core or a Switch core.

The UALink physical interface is a high bandwidth 200GT/s per Lane, maximum 4 Lanes, point-to-point serial interface Link between Accelerators and Switches, promoting a switching ecosystem for Accelerators. The UALink allows for up to 1024 Accelerators or endpoints in a network to communicate using a 10-bit Identifier.

MindShare’s UALink Fundamentals course provides a high-level understanding of the architecture of and AI computer platform consisting of Hosts, Accelerators with HBM Memory and Switches. We help you understand the specification terminology and definitions. We give you a high-level understanding of the function of each of the layers: Protocol, Transaction, Data Link and Physical Layers. Then, we describe the role of a UALink Switch.

You Will Learn:

- UALink spec terminology
- Function of each layer that makes up the UALink port stack
- UPLI interface overview
- UALink RAS support overview
- UALink Switch architecture overview

Course Length: 1 Day (or 2 half-days)

Who Should Attend: Engineering managers and designers looking to understand basic features and capabilities of UALink.

Course Outline:

Topics	1-Day Class
	UALink Fundamentals
UALink Features and Architecture Overview	
Accelerator System Node and Multi-Node architecture	X
UPLI and Stack Layers overview	X
Address Translation Model	X
RAS overview	X
UALink Switch overview	X

Recommended Prerequisites:

Computer architecture fundamentals. Suggested knowledge of high-speed serial bus architectures such as PCIe

Course Material:

- 1) Downloadable PDF version of the presentation slides
- 2) UALink Fundamentals eLearning course when available