

Ultra Accelerator Link (UALink) Architecture

Let MindShare Bring “Ultra Accelerator Link (UALink) Architecture” to Life for You

The UALink specification outlines a set of protocols and interfaces designed to form systems using multiple System Nodes aimed at AI applications. Each System Node normally includes one or more Host CPUs and Accelerators connected by various interconnects such as CXL, PCIe, AMD Infinity Fabric, etc. These nodes typically allow coherent access across Host and Accelerator memory within the node. Each node operates under a single OS image. UALink supports low-latency communication between Accelerators across System Nodes, allowing direct read, write, and atomic transactions. This inter-node communication is restricted to Accelerator initiated traffic. UALink protocol does not permit Host CPU access to memory across different System Nodes.

The UALink specification defines the UALink interface between different physical devices connected by a Link. The specification not only includes the traditional description of a serial bus stack (Transaction, Data Link and Physical Layer), but also includes a description of a UALink Protocol Level Interface (UPLI) also referred to as the Protocol Layer. The UPLI facilitates the standardization of an interface between a component and the UALink stack whether the component be an Accelerator core or a Switch core.

The UALink physical interface is a high bandwidth 200GT/s per Lane, maximum 4 Lanes, point-to-point serial interface Link between Accelerators and Switches, promoting a switching ecosystem for Accelerators. The UALink allows for up to 1024 Accelerators or endpoints in a network to communicate using a 10-bit Identifier.

MindShare’s comprehensive UALink 1.0 Architecture course provides a solid foundation of platform architectures and use cases of the UALink protocol. The course details the role of each of the layers in the stack. These include the Protocol Layer, Transaction Layer, Data Link Layer and Ethernet PHY Layer. We explain UALink Address Translation Model, Remote Memory Access (RMA) and UALink IO Coherency Model, UPLI operating rules, RAS, manageability and UALink Switch architecture, including configuration.

You Will Learn:

- UALink spec terminology
- Function of each layer that makes up the UALink port stack
- UPLI interface definitions and operating rules along with interface signals
- Tx and Rx compression caches
- TL Flit and Half Flit formats as well as DL Flit format
- DL message format
- TL Flow Control and DL Replay support
- Physical Layer encode/decode and FEC plus transmit and receive functions
- UALink RAS support
- Reset, signaling and connection
- Manageability requirements
- UALink Switch architecture and routing schemes

Course Length: 3 Days

Who Should Attend: This course is hardware-oriented but is suitable for both hardware design and software engineers. The course is ideal for RTL-, chip-, system- or system board-level design, verification and validation engineers who need a broad and in-depth understanding of UALink system architecture.

Course Outline:

Topics	3-Day Class	1-Day Class
	UALink 1.0	UALink Fundamentals
UALink Features and Architecture Overview		
Accelerator System Node and Multi-Node architecture	X	X
UPLI and Stack Layers overview	X	X
Address Translation Model	X	X
RAS overview	X	X
UALink Switch overview	X	X
UPLI and Protocol Layer		
UPLI Interface and Interface Signals	X	
Requests and Response paths	X	
Time Division Multiplexing	X	
UPLI Flow Control	X	
UPLI Transactions	X	
Ordering Rules for Read and Write Requests and Responses	X	
Transaction Layer		
TL features	X	
TL Flit and Half Flit formats, sequencing and packing	X	
TL Write Flit Sequence Encoding	X	
Tx and Rx Compression Caches	X	
TL Flow Control and Backoff Modes	X	
Data Link Layer		
DL features	X	
DL Flit formats and packing	X	
DL Messages	X	
Transmitter Pacing	X	
Link Level Replay	X	
DL States and Errors	X	
Physical Layer		
PL features	X	
Reconciliation Sublayers	X	
PCS/PMA modifications	X	
PCS and FEC	X	
Low Latency FEC Interleave	X	
UPLI Reset, Signaling and Connection		
UPLI Reset and Signaling	X	
UPLI Control	X	
RAS and Error Handling		
RAS requirements and End-to-End Data Protection	X	
RAS error types	X	
RAS error handling	X	
Manageability		
For Accelerators and System Nodes	X	
For Switches and Switch Platforms	X	
For Pod Controllers and Virtual Pods	X	
Manageability Workflows	X	
UALink Switches		
Bifurcation support	X	
Lossless Request and Response delivery	X	
Non-blocking architecture	X	
Forward progress guarantee	X	
Ordering Rules and Virtual Channels	X	
Routing Table structure	X	
Configuration	X	
Switch debug recommendations and Latency/Performance goals	X	



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Recommended Prerequisites:

Computer architecture fundamentals. Suggested knowledge of high-speed serial bus architectures such as PCIe

Course Material:

- 1) Downloadable PDF version of the presentation slides
- 2) UALink eLearning course when available

